DOI: 10.15514/ISPRAS-2020-32(2)-10

On reduced forms of initialized Finite State Machines with timeouts

[1] *A.S. Tvardovskii, ORCID: 0000-0001-7705-7214 <tvardal@mail.ru>*
[2,3] *N.V. Yevtushenko, ORCID: 0000-0002-4006-1161 <evtushenko@ispras.ru>*
[1] *National Research Tomsk State University,*
36, Lenin Ave, Tomsk, 634050, Russia
[2] *Ivannikov Institute for System Programming of the Russian Academy of Sciences,*
25, Alexander Solzhenitsyn st., Moscow, 109004, Russia
[3] *National Research University Higher School of Economics,*
20, Myasnitskaya st., Moscow, 101000, Russia

Abstract. Trace models such as Finite State Machines (FSMs) are widely used in the area of analysis and synthesis of discrete event systems. FSM minimization is a well-known optimization problem which allows to reduce the number of FSM states by deriving the canonical form that is unique up to isomorphism. In particular, the latter is a base for FSM-based 'black-box' test derivation methods such as W-method and its modifications. Since nowadays the behavior of many software and hardware systems significantly depends on time aspects, classical FSMs are extended by clock variables including input and output timeouts. The minimization of a Timed Finite State Machine (TFSM) includes both state and time aspects reduction. Existing approaches allow to derive the canonical representation for non-initialized deterministic TFSMs while for initialized TFSMs, i.e., TFSMs with the designated initial state, several pair-wise non-isomorphic minimal forms can exist. In this paper, we determine initialized TFSM classes for which the minimal form is unique up to isomorphism.

Keywords: Timed Finite State Machines; minimization; timeouts; initialized TFSM.

For citation: Tvardovskii A.S., Yevtushenko N.V. On reduced forms of initialized Finite State Machines with timeouts. Trudy ISP RAN/Proc. ISP RAS, vol. 32, issue 2, 2020. pp. 125-134. DOI: 10.15514/ISPRAS–2020–32(2)–10

Acknowledgements. This work is partly supported by RFFR Project No. 19-07-00327.

О минимизации инициальных автоматов с таймаутами

[1] *А.С. Твардовский, ORCID: 0000-0001-7705-7214 <tvardal@mail.ru>*
[2,3] *Н.В. Евтушенко, ORCID: 0000-0002-4006-1161 <evtushenko@ispras.ru>*
[1] *Национальный исследовательский Томский Государственный университет,*
634050, Россия, г. Томск, пр. Ленина, д. 36
[2] *Институт системного программирования им. В.П. Иванникова РАН,*
109004, Россия, г. Москва, ул. А. Солженицына, д. 25
[3] *Национальный исследовательский университет «Высшая школа экономики»,*
101000, Россия, г. Москва, ул. Мясницкая, д. 20

Аннотация. Модели с конечным числом состояний широко используются при решении задач анализа и синтеза дискретных систем, и минимизация конечных автоматов является известной проблемой оптимизации, которая позволяет уменьшить количество состояний конечного автомата, описывающего поведение дискретной системы, на основе использования его приведенной формы. Такая форма

единственна с точностью до изоморфизма для классических конечных автоматов, что, в частности, является основой для соответствующих методов синтеза тестов с гарантированной полнотой относительно «черного ящика», таких как W-метод и его модификации. Поскольку поведение современного программного и аппаратного обеспечения зачастую зависит от временных аспектов, в настоящее время классические автоматы расширяются временной переменной и связанными с ней входными и выходными таймаутами. Существующие подходы к минимизации временных автоматов охватывают оптимизацию как состояний, так и временных аспектов, и позволяют получить единственную минимальную форму для неинициальных детерминированных временных автоматов. В то же время для инициальных временных автоматов, т.е. автоматов с выделенным начальным состоянием, могут существовать различные попарно неизоморфные минимальные формы. В настоящей работе мы определяем классы инициальных временных автоматов, для которых минимальная форма единственна с точностью до изоморфизма.

Ключевые слова: временные автоматы; минимизация; таймауты; инициальные автоматы

Для цитирования: Твардовский А.С. Евтушенко Н.В. О минимизации инициальных автоматов с таймаутами. Труды ИСП РАН, том 32, вып. 2, 2020 г., стр. 125-134 (на английском языке). DOI: 10.15514/ISPRAS–2020–32(2)–10

Благодарности: Работа выполнена при частичной поддержке гранта РФФИ № 19-07-00327.

1. Introduction

Finite State Machines (FSM) [1, 2] are widely used for synthesis and analysis of discrete components of telecommunication and other hardware and software systems [3, 4, 5]. The complexity of solving many problems significantly depends on the number of states of an FSM that represents the system (component) specification; moreover, having the canonical form of a model usually simplifies solving these problems. For example, almost all FSM-based test derivation methods [6, 7] with guaranteed fault coverage for telecommunication protocols and other control systems with deterministic behavior are developed for reduced FSMs, i.e., FSMs which have different behavior at any two different states and such a reduced machine is unique for any complete deterministic FSM.

In the classical FSM theory, FSM minimization methods are well developed [1], i.e., given a deterministic complete FSM, it is well known how to derive a reduced form of the FSM that in fact is the canonical representation of a complete deterministic FSM. Nowadays time aspects become very important when describing the behavior of digital and hybrid systems, and, respectively, classical FSMs have been extended with time variables [see, for example, 8, 9, 10, 11]. A timed FSM (TFSM) is an FSM annotated with a *clock* and extended by input/output timeouts and input/output timed guards [10, 12]. Input timed guards describe the behavior at a given state for inputs which arrive during an appropriate time interval until timeout at the state expires. If no input is applied until the clock value reaches an (input) timeout then the system can spontaneously move to another state. An output timeout describes how long an applied input is processed at a given state. In the number of cases [10], an FSM with output timed guards is considered when an interval of possible output delays for processing each transition is given. In this paper, we assume that every output timeout is a non-negative integer. As a simple example, computers or mobiles can be considered when the devices move to a sleep mode if no button is pressed during an appropriate number of time units, i.e., no input is applied.

When minimizing classical FSMs (and other trace models) most attention is paid to minimizing the number of states of the machine under investigation. Differently from classical FSMs, a timed FSM can have several non-isomorphic state reduced forms and time aspects should be also taken into account when minimizing a TFSM. In [13], the notion of a time and state reduced non-initialized FSM with timed guards and timeouts is introduced. The authors also show that such minimal form is unique up to isomorphism for a non-initialized complete TFSM. However, such minimal form is not unique for an initialized complete FSM with timeouts while such machines are widely used for modeling timed systems with a reliable reset signal. For example, a number of test derivation

techniques are developed for initialized FSMs and the absence of the unique reduced form for Timed FSMs do not allow to directly apply W-methods and its derivatives to initialized TFSMs [14].

It is known that the reason for having several minimal forms is closely related to input timeouts [15], since for FSMs with timed guards there is the unique state and time reduced FSM with time guards [16]. In this paper, we determine classes of initialized FSMs with timeouts for which the unique minimal form can be derived.

The structure of the paper is as follows. Section 2 contains the preliminaries for classical and timed FSMs. In Section 3, the related work on minimizing TFSMs is briefly described. In Section 4, we determine a class of initialized TFSMs for which the minimal form is unique up to isomorphism. In Section 5, we show how the unique form can be derived for an FSM with timeouts based on its transformation to an FSM with timed guards. Section 6 concludes the paper.

2. Preliminaries

This section contains basic definitions of classical and timed Finite State Machines.

2.1 Finite State Machines

The model of a Finite State Machine (FSM) [1] is used for describing the behavior of a system that moves from state to state under input stimuli and produces predefined output responses. If the system has a reliable reset then usually the system behavior is described by an initialized FSM, i.e., by an FSM with the designated initial state. Formally, an initialized FSM is a 5-tuple $\mathsf{S} = (S, I, O, h_\mathsf{S}, s_0)$ where S is a finite non-empty set of states with the designated initial state s_0, I and O are input and output alphabets, and $h_\mathsf{S} \subseteq (S \times I \times O \times S)$ is the transition (behavior) relation. A transition (s, i, o, s') describes the situation when an input i is applied to S at the current state s and S moves to state s' and produces the output (response) o.

A trace or an *Input/Output sequence* α/γ of the FSM S at state s is a sequence of consecutive input/output pairs starting at the state s. There is a trace $\alpha/\gamma = i_1/o_1, i_2/o_2, \ldots, i_n/o_n$ at state s of FSM S if and only if there exist transitions $(s, i_1, o_1, s_1), (s_1, i_2, o_2, s_2), \ldots, (s_{n-1}, i_n, o_n, s_n)$. Given a trace α/γ, α is the *input projection* of the trace (input sequence) while γ is the corresponding *output projection* (output sequence), i.e., an output response of the FSM when the input sequence α is applied at state s. In this paper, if the converse is not explicitly stated, we consider *complete* and *deterministic* FSMs where for each state s and input sequence α there exists a single trace α/γ. Given an input sequence α of a deterministic complete FSM, state s' is the α-successor of state s in FSM S if S moves from state s to state s' when α is applied. Given an initialized FSM S, a trace α/γ is a trace of the FSM if it is a trace at the initial state of S.

2.2 Timed Finite State Machines

In this paper, a Timed FSM (TFSM) is an FSM with timeouts that can spontaneously move to another state when the timeout expires at a current state. Respectively, a TFSM is an FSM annotated with a clock (timed variable) and timeouts. A good example is a server implementation which can decline the connection when a client request is not applied within an appropriate timeout. Correspondingly, an initialized TFSM is a 6-tuple $\mathsf{S} = (S, I, O, h_\mathsf{S}, \Delta_\mathsf{S}, s_0)$ where S is a finite non-empty set of states with the designated initial state s_0, I and O are input and output alphabets, $h_\mathsf{S} \subseteq S \times I \times O \times S \times Z$ is the *transition relation*, Δ_S is the timeout function and Z is a set of *output delays* which are nonnegative integers. We consider the *timeout function* Δ_S: $S \to S \times (N \cup \{\infty\})$ where N is the set of positive integers: for each state this function specifies the maximum time for waiting for an input. If no input is applied until an (input) timeout expires then the system can spontaneously move to another state. By definition, for each state of the TFSM exactly one timeout is specified. An output delay describes the number of ticks when an output has to be produced after applying an input. A transition (s, i, o, s', d) describes the situation when an input i is applied to S

at the current state s. In this case, the FSM moves to state s', the clock value then is set to zero and S produces output o after d time units. Given state s of TFSM S such that $\Delta_\mathsf{S}(s) = (s', T)$, if no input is applied before the timeout T expires then the TFSM S moves to state s' while the clock value is set to zero. If $\Delta_\mathsf{S}(s) = (s', \infty)$ then $s' = s$; in other words, in this case, the TFSM can stay at state s infinitely long waiting for an input.

In this work, we consider *complete* and *deterministic* TFSMs where for each pair $(s, i) \in S \times I$, there exists a single transition $(s, i, o, s', d) \in h_\mathsf{S}$.

Similar to [7], for each state s of TFSM S we consider the function $time(s, t) = s'$ that determines state s' that will be reached by the TFSM if no input is applied during t time units.

A *timed input* is a pair (i, t) where $i \in I$ and t is a real; a timed input (i, t) means that input i is applied to the TFSM at time instance t. A timed output is a pair (o, d) where $o \in O$ and d is the output delay. A sequence of timed inputs $\alpha = (i_1, t_1) \ldots (i_n, t_n)$ is a *timed input sequence*, a sequence of timed outputs $\gamma = (o_1, d_1) \ldots (o_n, d_n)$ is a *timed output sequence*. A sequence $\alpha/\gamma = (i_1, t_1)/(o_1, d_1) \ldots (i_n, t_n)/(o_n, d_n)$ of consecutive pairs of timed inputs and timed outputs starting at the state s is a *timed I/O sequence* or a *timed trace* of TFSM S at state s. Similar to FSMs, α is an applied timed input sequence while γ is the corresponding output response of the TFSM to sequence α of applied inputs. The behavior of TFSM S at state s is the set of all timed traces at this state. For a timed input sequence α of TFSM S at state s the α-successor is defined similar to FSM.

In order to determine the output response of the TFSM at state s to a timed input (i, t), state $s' = time(s, t)$ is calculated first. State s' is a state where the TFSM moves from state s via timeout transitions such that the maximum sum Σ of all timeouts starting from state s is less than t and $t - \Sigma < T$, where $\Delta_\mathsf{S}(s) = (s''', T)$. At the second step, a transition (s', i, o, s'', d) is used and respectively, the machine produces the output (o, d) to a timed input (i, t) applied at state s and moves to the next state s''. Thus, the output response of the TFSM to a timed input sequence at state s is iteratively determined starting from state s. Similar to FSMs, the set of all timed traces at the initial state of the initialized TFSM determines the TFSM behavior.

A timed input sequence α is a *transfer* sequence for state s or simply an *s-transfer* sequence in TFSM S if state s is the α-successor of the initial state of S. If for state s of TFSM S there exists a *transfer* timed input sequence α, then s is an *input-reachable* state, otherwise s is *input-unreachable*. By default, the initial state is input-reachable, since it is reachable by the empty input sequence. If for an input-unreachable state s' there exists a time instance t and *input-reachable* state s such that $time(s, t) = s'$ then s' is time-reachable. The TFSM S is initially *connected* or simply *connected* if each state $s \in S$ is input- or time-reachable. In this paper, we consider only connected TFSMs.

Example. Consider a TFSM S in Figure 1 with the initial state a. This TFSM is connected but state b is input-unreachable.

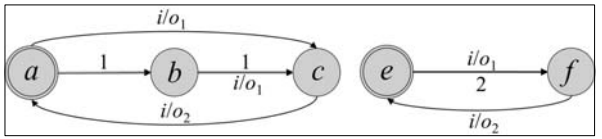

Fig. 1. State and time reduced equivalent initialized TFSMs S with the initial state a (on the left) and P with the initial state e (on the right)

Рис. 1. Приведённые по состояниям и времени инициальные временные автоматы S (слева) и P (справа) с начальными состояниями a и e соответственно

3. Minimization problem

There is a big body of work for minimizing a classical deterministic complete FSM based on the state equivalence [1]. We now remind the notion of equivalent states for deterministic complete (Timed) FSMs [1, 12]. Given complete deterministic (Timed) FSMs S and P with their states s

and p, states s and p are *equivalent* if (timed) output responses at these states coincide for each (timed) input sequence. If states s and p are not equivalent then they are *distinguishable*. Initialized (Timed) FSMs are *equivalent* if their initial states are equivalent. Equivalent (Timed) FSMs have the same behavior. Two TFSMs S and P are *isomorphic* if there exists the one-to-one correspondence H: $S \to P$ such that there exists a transition $(s, i, o, s', d) \in h_S$ if and only if there exists a transition $(H(s), i, o, H(s'), d) \in h_P$ and $\Delta_P(H(s)) = (H(s'), T)$ if and only if $\Delta_S(s) = (s', T)$. A complete deterministic (Timed) FSM S is *state reduced* if every two different states s_1, $s_2 \in S$ are not equivalent.

3.1 FSM Minimization

The minimal form of a (initialized) deterministic complete FSM S is defined as a (initialized) state reduced FSM which is equivalent to S. An algorithm for deriving the minimal form (or an FSM minimization algorithm) for classical deterministic complete FSMs has been proposed in [1] and is based on partitioning the state set into equivalence classes, i.e., subsets with pairwise equivalent states. The equivalence relation induces a partition E of the set of states of a complete deterministic FSM. Any two states of the same class of the partition E are equivalent; any two states of different classes of partition E are distinguishable. Respectively, states of the reduced form correspond to classes of the partition E, i.e., the number of states of the reduced form equals the cardinality of E. The transition relation of the reduced form is derived based on transitions between E classes. It is shown that the minimal form of an initialized FSM as well as of a non-initialized deterministic complete FSM is unique up to isomorphism.

3.2 TFSM Minimization

The notions of a state reduced TFSM and the partition into equivalent states are defined similar to those of classical FSMs. A state reduced form of an FSM with timeouts can be derived based on its FSM abstraction [13, 15]. Moreover, in order to derive the unique minimal form up to isomorphism for a non-initialized FSM with timeouts, a so-called time reduced form should be also constructed.

A non-initialized FSM with timeouts S is *time reduced* if for each state s such that $\Delta_S(s) = (s', T)$, it holds that for each state $s'' \in S$ and integer $T' < T$, TFSM S′ which is obtained from S by replacing the timeout at state s to $\Delta_S(s) = (s'', T')$, is not equivalent to S. Minimal timeouts for states of TFSM S can be found based on its FSM abstraction [13]. In other words, when deriving a time reduced form of a non-initialized TFSM, the timeout for each state s should be set to the minimum value in such a way that the TFSM behavior at state s is not changed.

In [13], the following theorem has been proven.

Theorem 1. Two non-initialized deterministic complete state and time reduced FSMs with timeouts are equivalent if and only if they are isomorphic.

Respectively, the minimal form of a non-initialized deterministic complete TFSM is unique up to isomorphism.

3.3 The uniqueness of the minimal form of initialized FSMs with timeouts

Unlike non-initialized Timed FSMs, a complete deterministic initialized FSM with timeouts can have several non-isomorphic state and time reduced forms. An example is shown in Figure 1 where two equivalent minimal initialized FSMs with timeouts are presented. However, those TFSMs are not isomorphic. The reason is that for non-initialized equivalent TFSMs, for each state of one machine there is an equivalent state of another machine and vice versa. For initialized machines it is not the case for input-unreachable states.

In fact, there can exist some states in TFSMs which are only time-reachable, i.e., are not input-reachable, for example, state b of TFSM S (Figure 1). This input-unreachable state can be removed from the TFSM if the TFSM moves from state a to state c via a timeout transition. The corresponding

TFSM P is presented in the Figure 1 on the right where the timeout of value two is used instead of two timeouts of value one. Therefore, the problem that a reduced form of an FSM with timeouts is not unique is closely related to states which are only time-reachable because for these states, the requirement for the one-to-one correspondence between states of initialized equivalent TFSMs does not need to necessarily hold. In this paper, we specify classes of initialized FSMs with timeouts for which the state and time reduced form is unique up to isomorphism.

4. Input-connected FSM with timeouts

Since the existence of several state and time reduced equivalent but non-isomorphic initialized FSMs with timeouts is closely related to time-reachable states, we first consider TFSMs without such states.

An FSM with timeouts S is *input-connected* if each state $s \in S$ is input-reachable. In other words, given a state s of an input-connected initialized FSM with timeouts, there exists a transfer timed input sequence from initial state to state s. For input-connected TFSMs, the following proposition can be proven.

Proposition 1. Two deterministic complete state and time reduced initialized input-connected FSMs with timeouts are equivalent if and only if they are isomorphic.

Proof. Let deterministic complete state and time reduced initialized input-connected FSMs S and P with timeouts be equivalent. Since the TFSMs are equivalent then α-successors s and p of initial states TFSMs S and P respectively are equivalent for any timed input sequence α. Moreover, since S and P are state reduced then one-to-one correspondence H_i: $S \to P$ can be established such that $p = H_i(s)$ is an input-reachable state of TFSM P which is equivalent to the input-reachable state s. Similar to [13], for each transition $(s, i, o, s', d) \in h_S$ there exists a transition $(H_i(s), i, o, H_i(s'), d) \in h_P$. Let there exist a pair of states s and $p = H_i(s)$ such that $\Delta_S(s) = (s', T_s)$ and $\Delta_P(p) = (p', T_p)$ and $T_p < T_s$. Due to the fact that S and P are equivalent, there exists state s'' which is equivalent to state $p' = H_i(s'')$. Since states s and p are also equivalent, the timeout at state s can be replaced by $\Delta_S(s) = (s'', T_s')$ where $T_s' = T_p < T_s$. The latter is not possible as S is time reduced. Since P is time reduced too, the same reasoning can be applied when $T_s < T_p$ and thus, $T_s = T_p$. Since states s and p are equivalent, states $time(s, T_s)$ and $time(p, T_p)$ are also equivalent and respectively, $p' = H(s')$. Thus, $\Delta_P(H_i(s)) = (H_i(s'), T)$ if and only if $\Delta_S(s) = (s', T)$.

Since isomorphic TFSMs coincide up to state renaming, isomorphic TFSMs are equivalent.

Corollary. The minimal (state and time reduced) form of an input-connected initialized FSM with timeouts is unique up to isomorphism.

However, there exist FSMs with timeouts which have time-reachable states, i.e., are not input-connected. We next consider such TFSMs and discuss when the unique minimal form for TFSMs with input-unreachable states can be derived.

5. Minimization procedure using FSMs with timed guards

Given an FSM with timeouts, according to the corollary to Proposition 1, if this FSM has a state and time reduced input-connected form, then this form is unique up to isomorphism. However, just now we do not know whether such a minimal form exists for any FSM with timeouts. On the other hand, FSMs with timed guards can be considered as another type of the minimal form and such TFSMs are input-connected. It is known [12] that there exists a class of FSMs with timeouts which can be represented by a corresponding FSM with timed guards. Respectively, in this section, we show that if for an FSM with timeouts there exists a minimal form with timed guards then such minimal form is unique up to isomorphism.

5.1 FSM with timed guards

An initialized FSM with timed guards is a 5-tuple $\mathsf{S} = (S, I, O, s_0, h_\mathsf{S})$ where I and O are input and output alphabets, S is the finite non-empty set of states with the designated initial state s_0, $h_\mathsf{S} \subseteq (S \times I \times O \times S \times \Pi \times Z)$ is the *transition relation* with the set of *input timed guards* Π. An input timed guard $g \in \Pi$ describes the time domain when a transition can be executed and is given in the form of interval $\lceil min, max \rceil$ from $[0; \infty)$, where $\lceil \in \{(, [\}, \rceil \in \{),]\}$. The transition $(s, i, o, s', g, d) \in S \times I \times O \times S \times \Pi \times Z$ means that TFSM S being at state s accepts an input i applied at time $t \in g$ measured from the moment when TFSM S entered state s; the clock then is set to zero, S produces output o and moves to state s' after d time units.

The state reduced form for FSM with timed guards can be derived based on its FSM abstraction [13] or by the algorithm presented in [16]. Moreover, an FSM with timed guards is *time reduced* if for each two transitions $(s, i, o, s', g_1, d), (s, i, o, s', g_2, d) \in h_\mathsf{S}$ it holds that timed guards g_1 and g_2 cannot be merged into a single guard. Thus, in order to derive the time reduced form for an FSM with timed guards, transitions under the same input with the same output and output delay, between the same states, the timed guards which can be merged should be replaced by a single transition. The uniqueness of the minimal form of a non-initialized FSM with timed guards has been proven in [13] and next we formulate a similar proposition for initialized TFSMs.

Proposition 2. Two deterministic complete time and state reduced initialized connected FSMs with timed guards are equivalent if and only if they are isomorphic.

Proof. Let deterministic complete time and state reduced initialized connected FSMs with timed guards S and P be equivalent. Since TFSMs S and P are equivalent, the α-successors s and p of initial states of these TFSMs are also equivalent for each α, i.e., at these states there are the same output responses for each timed input sequence. Moreover, since S and P are state reduced then the one-to-one correspondence H: $S \to P$ can be established such that $p = H(s)$ is a state of TFSM P which is equivalent to state s. We now show that for each transition $(s_1, i, o, s_2, g, d) \in \lambda_\mathsf{S}$ there exists a transition $(p_1, i, o, p_2, g, d) \in \lambda_\mathsf{P}$, where $p_1 = H(s_1)$ and $p_2 = H(s_2)$. Let there exist $(s_1, i, o, s_2, g, d) \in \lambda_\mathsf{S}$, but $(H(s_1), i, o, H(s_2), g, d) \notin \lambda_\mathsf{P}$. Since s_1 and p_1 are equivalent, the behavior of P at state p_1 in time interval g coincides with that of the TFSM S at state s_1. Respectively $(p_1, i, o, p_2, g', d) \in \lambda_\mathsf{P}$, where $g \subset g'$, because P is state and time reduced. However, the behavior of TFSM S for the same input i at state s for time instances in g differs from that in adjacent intervals since S is state and time reduced. Thus, there exists $t \in g' \setminus g$, such that the output responses to (i, t) at states s and p do not coincide. In a similar way, we can show that for each transition $(H(s_1), i, o, H(s_2), g, d) \in \lambda_\mathsf{P}$ there exists a transition $(s_1, i, o, s_2, g, d) \in \lambda_\mathsf{S}$ and thus, S and P are isomorphic.

Since isomorphic TFSMs coincide up to state renaming, isomorphic TFSMs are equivalent.

Thus, the minimal (state and time reduced) form of an initialized FSM with timed guards is unique up to isomorphism and next we show how FSM with timeouts can be represented by a TFSM with timed guards in some cases.

5.2 Transformation of an FSM with timeouts into an FSM with timed guards

An FSM with timeouts S is *timeout loop-free* [12] if there is no cycle of transitions labeled with timeouts. A timeout loop-free FSM can be represented as an FSM with timed guards by the algorithms proposed in [12].

Algorithm 1: Transforming a timeout loop-free FSM into an FSM with timed guards

Input: A timeout loop-free FSM $\mathsf{S}' = (S, I, O, h_\mathsf{S}, \Delta_\mathsf{S}, s_0)$

Output: The FSM with timed guards S

While there exists $s_j \in S$ such that $\Delta_\mathsf{S}(s_j) = (s_k, T)$, $T < \infty$ **do**

for each $(s_k, i, [t_1, t_2), o, s_h, d) \in h_\mathsf{S}$ **do** $h_\mathsf{S} = h_\mathsf{S} \cup \{(s_j, i, [t_1 + T, t_2 + T), o, s_h, d)\}$;

if $\Delta_\mathsf{S}(s_k) = (s_f, T_f)$ **then** $\Delta_\mathsf{S}(s_j) = (s_f, T_f + T)$ **else** $\Delta_\mathsf{S}(s_j) = (s_j, \infty)$;

Return $\mathsf{S} = (S, I, O, h_\mathsf{S}, s_0)$.

Proposition 3 [12]. Given a complete deterministic initialized timeout loop-free FSM S', let S be an FSM with time guards returned by Algorithm 1 for S'. TFSM S is a complete deterministic initialized FSM with timed guards that is equivalent to S'.

Let S be an FSM with timed guards that is returned by Algorithm 1 for a timeout loop-free FSM S'. Note that each time-reachable state of TFSM S' becomes unreachable from the initial state of TFSM S and, respectively, can be removed since the behavior at this state does not affect the machine behavior at the initial state. As an example, for the timeout loop-free FSM S in Figure 1 the corresponding FSM with timed guards Q is presented in Figure 2.

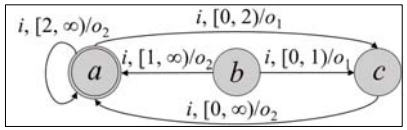

Fig. 2. An FSM with timed guards Q that is equivalent to FSM with timeouts S in Fig. 1
Рис. 2. Автомат с временными ограничениями Q, эквивалентный автомату с таймаутами S на рисунке 1

State b of TFSM Q becomes unreachable from the initial state a and can be removed without changing the initialized TFSM behavior. The following proposition can be proven based on Proposition 2 and results from [12].

Proposition 4. Two deterministic complete initialized timeout loop-free FSMs are equivalent if and only if corresponding state and time reduced FSMs with timed guards are isomorphic.

Given an initialized timeout loop-free FSM S, the state and time reduced form can be derived for S as such a form for a corresponding FSM with timed guards. Respectively, the unique minimal form for FSM with timed guards or timeouts P can be derived by the following algorithm.

Algorithm 2: Deriving the minimal form of an initialized FSM with timed guards or timeouts

Input: An initialized FSM with timed guards or an initialized FSM with timeouts S

Output: The minimal FSM with timed guards S'

Step 1. If S is an FSM with timeouts then Step 2, else Step 3.

Step 2. If S is a timeout loop-free FSM then call Algorithm 1 for deriving a corresponding FSM with timed guards and Step 3, else the unique minimal form as an FSM with timed guards cannot be derived.

Step 3. The unique minimal form with timed guards S' is derived as described in [16].

Proposition 5. Let P be a TFSM returned by the Algorithm 2 for a complete deterministic initialized timeout loop-free FSM or an FSM with timed guards S. TFSM P is a complete deterministic initialized state and timed reduced FSM with timed guards which is equivalent to S.

Given an FSM with timed guards or timeouts, we next determine a corresponding class of TFSMs with the unique minimal form in the following way.

Theorem 2. Given two deterministic complete FSMs with timed guards or timeouts S and P which are initialized connected timeout loop-free TFSMs, S and P are equivalent if and only if their time and state reduced forms of corresponding FSMs with timed guards are isomorphic.

6. Conclusion

In this work, we have investigated the uniqueness of the minimal form for initialized FSMs with timeouts. We determine two TFSM classes for which the minimal form is unique up to isomorphism. The first class contains initialized TFSMs for which all states are reachable from initial state under a timed input sequence. The second class contains TFSMs which are timeout loop-free, i.e., their transition diagrams have no loops labeled with timeouts.

We also note that the uniqueness of the minimal form for Timed FSMs allows to directly adapt classical W-based test derivation methods for TFSMs. These methods are based on checking the equivalence relation by checking the isomorphism (or possibly another relation for nondeterministic TFSMs) between the specification and an implementation under test. We also plan to study the possibility of deriving homing and synchronizing sequences for FSMs with timeouts based on their minimal forms.

References / Список литературы

[1]. A. Gill. Introduction to the Theory of Finite-State Machines, McGraw Hill, 1962, 207 p.

[2]. D. Lee, M. Yannakakis Principles and methods of testing finite state machines-a survey. Proceedings of the IEEE, vol. 84, no. 8, 1996, pp. 1090-1123.

[3]. T.E. Murphy, X.-J. Geng, and J. Hammer. On the control of asynchronous machines with races. IEEE Transactions on Automatic Control, vol. 48, no. 6, 2003, pp. 1073-1081.

[4]. Kumar Ratnesh, Garg Vijay K. Modeling and control of logical discrete event systems. The Springer International Series in Engineering and Computer Science, 1995, 143 p.

[5]. C. C. Cassandras, S. Lafortune. Introduction to discrete event systems. Springer, 1999, 828 p.

[6]. Rita Dorofeeva et al. FSM-based conformance testing methods: A survey an-notated with experimental evaluation. Information and Software Technology, vol. 52, issue 12, 2010, pp. 1286-1297.

[7]. Maxim Zhigulin, Nina Yevtushenko, Stéphane Maag, Ana R. Cavalli. FSM-Based Test Derivation Strategies for Systems with Time-Outs. In Proc. of the 11th International Conference on Quality Software, 2011, pp. 141-149.

[8]. Tripakis S. Folk theorems on the determinization and minimization of timed automata. Information Processing Letters, vol. 99, no. 6, 2006, pp. 222-226.

[9]. Merayo M., Nunez M., Rodriguez I. Formal testing from timed finite state machines, Computer Networks, vol. 52, issue 2, 2008, pp. 432-460.

[10]. Gromov M., El-Fakih K., Shabaldina N., and Yevtushenko N. Distinguishing non-deterministic timed fnite state machines. In Formal Techniques for Distributed Systems. Lecture Notes in Computer Science. vol. 5522, 2009, pp.137-151.

[11]. R.M. Hierons, M.G. Merayo, M. Nunez. Testing from a Stochastic Timed System with a Fault Model / // Journal of Logic and Algebraic Programming, vol. 72, issue 8, 2009, pp. 98-115.

[12]. Bresolin D., El-Fakih K., Villa T., Yevtushenko N. Deterministic Timed Finite State Machines: Equivalence Checking and Expressive Power. In Proc. of the 5th International Symposium on Games, Automata, Logics and Formal Verification (GandALF2014), 2014, pp. 203–216.

[13]. Tvardovskii A.S., Yevtushenko N.V., Gromov M.L. Minimizing Finite State Machines with time guards and timeouts. Trudy ISP RAN/Proc. ISP RAS, vol. 29, issue 4, 2017 г., pp. 139-154 (in Russian). DOI: 10.15514/ISPRAS-2017-29(4)-8 / Твардовский А.С., Евтушенко Н.В., Громов М.Л. Минимизация автоматов с таймаутами и временными ограничениями. Труды ИСП РАН, том 29, вып. 4, 2017 г., стр. 139-154.

[14]. Khaled El-Fakih, Nina Yevtushenko, Hacène Fouchal. Testing Timed Finite State Machines with Guaranteed Fault Coverage. Lecture Notes in Computer Science, vol. 5826, 2009. pp. 66-80.

[15]. Tvardovskiy A. On the minimization of timed Finite State Machines. Trudy ISP RAN/Proc. ISP RAS, vol. 26, issue 6, 2014, pp. 77-84 (in Russian). DOI: 10.15514/ISPRAS-2014-26(6)-7 / Твардовский А.С. К минимизации автоматов с таймаутами, том 26, вып. 6, 2014 г., стр. 77-84.

[16]. Tvardovskiy A.S., Yevtushenko N.V. Minimizing Timed Finite State Machines. Tomsk State University Journal of Control and Computer Science, № 4(29), 2014, pp. 77-83 (in Russian) / Твардовский А.С., Евтушенко Н.В. К минимизации автоматов с временными ограничениями. Вестник Томского государственного университета. Управление, вычислительная техника и информатика, 2014 г., № 4(29), стр. 77–83.

Information about authors / Информация об авторах

Aleksander Sergeevitch TVARDOVSKII received his Master's degree from Faculty of Radiophysics of Tomsk State University. He is a Ph.D. student at Tomsk State University since 2017. His research interests include automata theory and software testing.

Александр Сергеевич ТВАРДОВСКИЙ получил степень магистра радиофизики в ТГУ. С 2017 года обучается в аспирантуре ТГУ. Исследовательские интересы включают теорию автоматов и тестирование программного обеспечения.

Nina Vladimirovna YEVTUSHENKO, doctor of technical sciences, professor, a leading researcher of ISP RAS, worked at the Siberian Scientific Institute of Physics and Technology as a researcher up to 1991. In 1991, she joined Tomsk State University as a professor and then worked as the chair head and the head of Computer Science laboratory. Her research interests include formal methods, automata theory, distributed systems, protocol and software testing.

Нина Владимировна ЕВТУШЕНКО, доктор технических наук, профессор, г.н.с. ИСП РАН, до 1991 года работала научным сотрудником в Сибирском физико-техническом институте. С 1991 г. работала в ТГУ профессором, зав. кафедрой, зав. лабораторией по компьютерным наукам. Её исследовательские интересы включают формальные методы, теорию автоматов, распределенные системы, протоколы и тестирование программного обеспечения.