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Electrostatic Discharge Protection Devices Macromodelling Using Open-Source Tools

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Abstract. The semiconductor diode and grounded gate MOSFET (GGMOS) devices are commonly used as electrostatic discharge (ESD) protection element in CMOS ICs circuitry. This article presents an implementation of ESD diode and GGMOS macro models using open-source circuit simulation tools (Qucs-S and Ngspice). The proposed models could serve for the circuit simulation of the ESD event. Such simulation allows to estimate the ESD robustness of the IC at the early design stage.

Keywords: electrostatic discharge (ESD); circuit simulation; compact modelling; transmission line pulse.

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Макромоделирование компонентов защиты от электростатического разряда с применением программного обеспечения с открытым исходным кодом

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Аннотация. Полупроводниковый диод и полевой транзистор с заземлённым затвором (GGMOS) часто используются в качестве элементов защиты от электростатического разряда (ЭСР) в схемотехнике КМОП ИМС. В статье представлена реализация макромоделей данных компонентов с использованием ПО для схемотехнического моделирования с открытым исходным кодом. Предложенные модели могут служить для моделирования воздействия ЭСР на ИМС. Подобное моделирование позволяет оценить стойкость ИМС к воздействию ЭСР на ранней стадии проектирования.

Ключевые слова: электростатический разряд; схемотехническое моделирование; компактные модели; импульс линии передачи.

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1. Introduction

The ESD protection circuit is a part of all modern digital and analog CMOS ICs. There exists a number of proprietary specialized simulation tools like Cadence ESD Checker or Magwell ESDi for ESD stress modelling. Different semiconductor devices may be used for ESD proptection purpose. The aluminum gate CD4000 and polysilicon gate 74HC series has used the diode protection. The operating principle of the diode protection circuit is based on the properties of the p-n junction IV-curve (Fig. 1a). After reaching the first breakdown voltage V_{br} the diode acts as the voltage limiter until the thermal breakdown point (V_{t2}; I_{t2}) and device destruction. The diode ESD protection circuit could be simulated using the general purpose SPICE [1] diode model. But this approach has some disadvantages. The ESD protection operates in high current regions under short pulse duration. The diode body resistance may have a nonlinear dependency [2] on current that should be considered for typical ESD current range. The development of the diode macromodel taking into account ESD effects will improve the simulation accuracy.

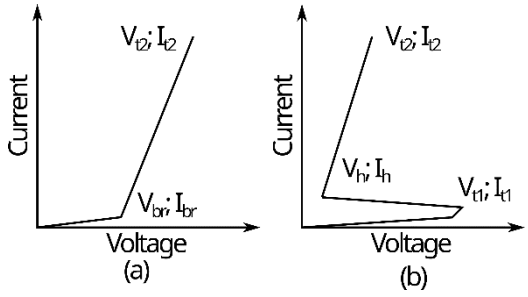

Fig. 1. Idealized IV-curves of diode (a) and the GGMOS (b) ESD protection devices.

The more modern digital IC series including submicron technology nodes used the ESD protection based on grounded gate MOSFET (GGMOS) device [3]. The operating principle of this ESD protection is based on the thyristor effect in the parasitic lateral BJT formed by drain, source, and channel regions of the MOSFET device. The cross-section of the MOSFET device is shown in the Fig. 2.

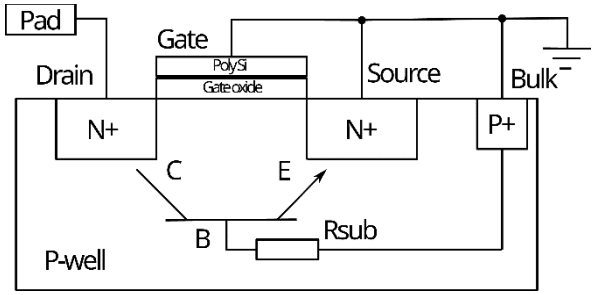

Fig. 2. Cross-section of the GGMOS ESD protection device.

The typical IV-curve of the GGMOS device is shown in the Fig. 1b. The parasitic BJT starts to conduct at the trigger voltage point V_{t1}, I_{t1}. Then the device latches up and voltage drops to the holding voltage V_h. If the current across the device exceeds the second breakdown point I_{t2}, the GGMOS device goes to the thermal breakdown and the protection is destroyed. The trigger voltage V_{t1} should not exceed the gate breakdown voltage for the proper device operation. This IV-curve could be obtained using quasi-static transmission line pulse (TLP) method.

The GGMOS device operation under ESD stress cannot be simulated using existing SPICE models. The MOS level 1-9 or BSIM [4] models don't take into account parasitic BJT behavior. The special macromodel is needed to simulate the GGMOS ESD protection with SPICE. A compact model of the GGMOS device has been proposed by J. Li, E. Rosenbaum and Y. Zhou [5], [6]. But the existing publications on this topic don't consider the practical implementation of the proposed model using the circuit simulation CAD tools and model parameters extraction.

The purpose of this research is to implement a practical ESD protection devices (diode and GGMOS) macromodels using the open-source circuit simulation tools (Qucs-S and Ngspice).

2. ESD diode macromodel

The proposed diode macromodel is shown in the Fig. 3. This model is designed using Qucs-S circuit simulation software with Nsgpice backend. The R_{tlp} behavioral resistance is connected in series to SPICE diode model. It represents the dependency of the diode resistance on the forward current.

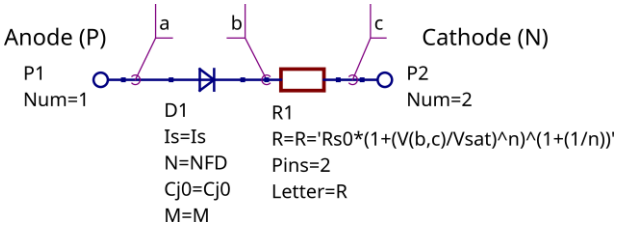

Fig. 3. Diode macromodel taking into account ESD effects.

The model uses the following dependency of the diode resistance on current:

$$R_{tlp} = R_{s0}\left(1+\left(\frac{V}{V_{sat}}\right)^{n}\right)^{\left(1+\frac{1}{n}\right)} \quad (1)$$

where the V is the voltage drop across the series resistance. Other symbols are the model parameters and explained in the Table 1.

Table 1. ESD diode model parameters.

Parameter	Description	Default value
V_{sat}	saturation voltage (V)	1.0
R_{s0}	initial diode series resistance (Ohm)	1.0
N	fitting coefficient N > 1	1.02

As could be seen, the model requires three additional parameters except the standard SPICE diode parameters. The R_{s0} resistance could be extracted from the TLP IV-curve of the diode (Fig. 1a) as the differential resistance at the initial part between V_{br} and V_{t2}. The remaining parameters could be extracted from the measurements data using the curves fitting.

The Fig. 4 shows the DC sweep simulation result for general SPICE diode model and improved ESD diode macromodel. The model parameters were extracted to match the TLP measurement data for drain-bulk diode in the MOSFET device. The TLP setup designed by authors was used for the measurements [7,8]. The gate dielectric degradation after the ESD stress could be investigated using the methods presented in [9]. The improved macromodel shows the better matching than SPICE model. The testbench schematic in Qucs-S CAD and model parameters are shown in the Fig. 5.

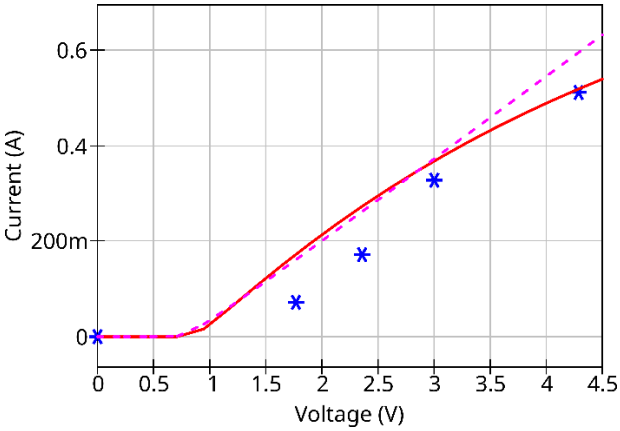

Fig. 4. Simulated (solid line) ESD diode IV-curve; general SPICE diode IV-curve (dashed line), and measured TLP diode IV-curve (stars).

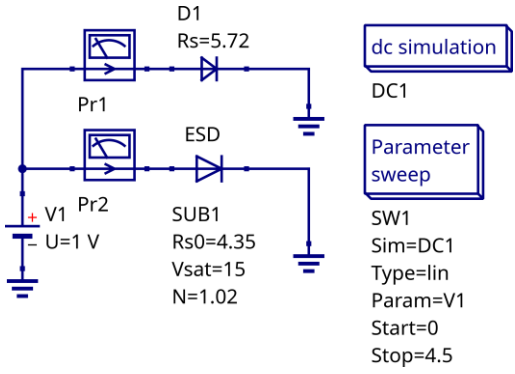

Fig. 5. Diode macromodel DC sweep testbench schematic. D1 – SPICE diode; SUB1 – improved micromodel.

3. GGMOS device macromodel

The equivalent circuit of the GGMOS device is shown in the Fig. 6. This macromodel was designed using Qucs-S [10,11] circuit simulation tool with Ngspice backend follows the model proposed in [5]. The parasitic NPN BJT is connected in parallels to NMOS device channel. The MOSFET uses level 1-9 model for micron technology or BSIM model for submicron technology. The BJT uses full Gummel-Poon model. The approach using the compact model (MOS level 1 and Ebers-Moll for BJT) was also tested, but the full SPICE model showed a better convergence for time domain simulation. The setting of the forward Early voltage (VAF) parameter of the BJT requires to improve the model convergence. Two additional current controlled current sources (CCCS) B1 and B2 are needed to simulate the impact ionization current Iii and triggering of the parasitic BJT. The resistor Rc represents drain area resistance, and Rsub represents the substrate resistance. The C1 capacitor is convergence helper. The Vc and Vd are the current sensing zero voltage sources.

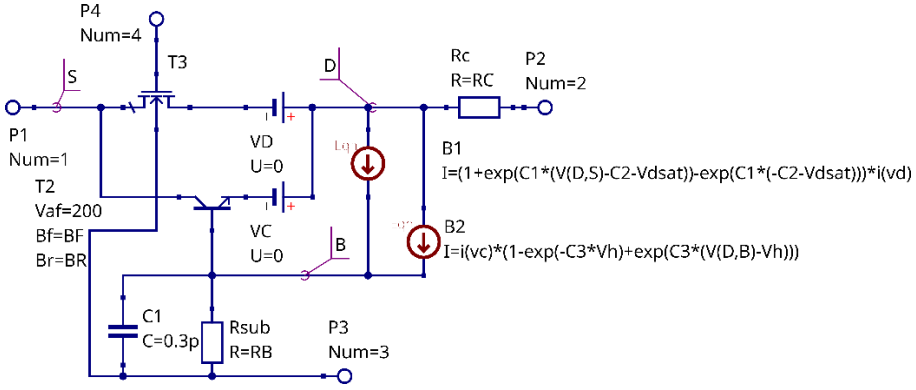

Fig. 6. GGMOS device equivalent circuit.

The impact ionization current depends on MOSFET drain I_d and BJT collector I_c currents as following:

$$I_{ii} = M_1 I_d + M_2 I_c \tag{2}$$

where the M1 and M2 are the multiplication factors that depends on device voltages as following:

$$M_1 = 1 + \exp\left(C_1\left(V_{ds} - C_2 - V_{dsat}\right)\right) - \exp\left(C_1\left(-C_2 - V_{dsat}\right)\right) \tag{3}$$

$$M_2 = 1 - \exp\left(-C_3 V_h\right) + \exp\left(C_3 V_{db} - V_h\right) \tag{4}$$

where V_{ds} is drain-source voltage; V_{db} is drain bulk voltage; the value of R_c could be extracted from the TLP IV-curve measurement (see Fig. 1) as the following:

$$R_c = R_{diff} = \frac{V_{t1} - V_h}{I_{t2} - I_h} \tag{5}$$

Other parameters in equations (3) and (4) are explained in the Table 2.

The C_1, C_2, and C_3 fitting coefficients are tuned to provide the equality of simulated and measured trigger voltage V_{t1} and trigger current I_{t1}.

4. GGMOS device simulation result

DC testbench schematic is shown in the Fig. 7. The current source sweep is used, because the IV-curve of the GGMOS device is a multivalued function and has a negative resistance part from trigger voltage V_{t1} to holding voltage V_h.

Table 2. GGMOS model parameters.

Parameter	Description	Default value
V_h	holding voltage (V)	extracted from IV-curve
V_{dsat}	saturation voltage (V)	1.0
C_1	fitting coefficient	2.0
C_2	fitting coefficient	2.0
C_3	fitting coefficient	2.0
B_F	parasitic BJT forward beta	2.0
B_R	parasitic BJT reverse beta	1.5
R_{sub}	substrate resistance (Ohm)	200
R_c	ON state resistance (Ohm)	5

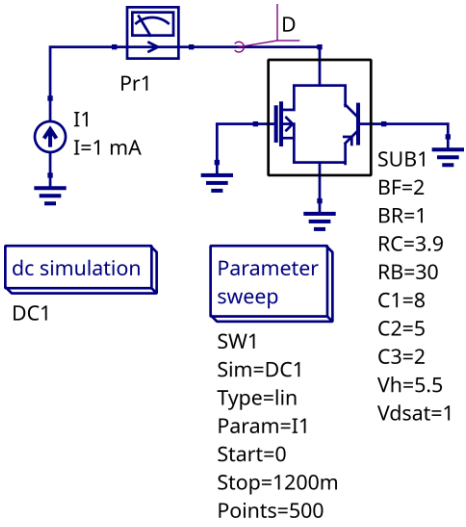

Fig. 7. GGMOS model DC testbench schematic.

The model parameters could be fitted to match the experimental TLP data (Fig. 8).

The simulated and measured data have a good match at the corner points (see the Table 3).

The trigger current I_{t1} has the highest mismatch. This could be explained by the low sensitivity of the used measurement setup when measuring the TLP currents around 10 mA. The mismatch of the negative resistance part slope have the following explanation. The V_h, I_h point for the measured curve lies on load line [12] that depends on the TLP setup output resistance Z_{tlp} and pulse voltage V_p on the source. The load line equations are the following:

$$I_{DUT} = \frac{V_p - V_{DUT}}{Z_{TLP}} \tag{6}$$

where V_{DUT} , I_{DUT} are the current and voltage across the device under test (DUT).

The simulation testbench schematic uses the current source having $Z_{tlp} = \infty$, so the slope of the load line for the DC sweep simulation and measurement will be different.

The transient simulation testbench schematic is shown in the Fig. 9. The pulsed voltage source represents the charged line. The Pi-attenuator circuits represents the output resistance of the TLP setup. The standard 100 ns pulse width is used.

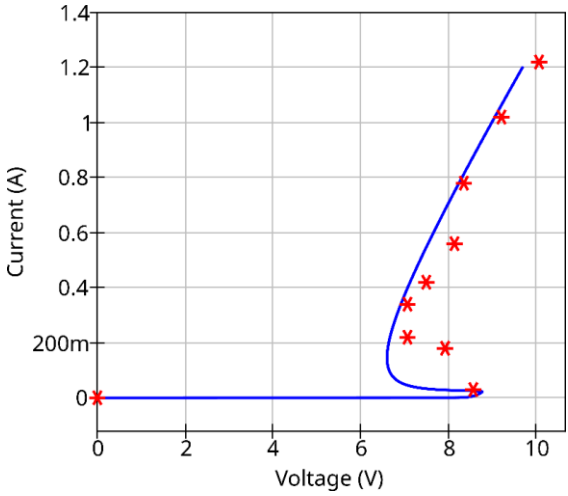

Fig. 8. GGMOS model simulated (solid line) and measured (stars) IV-curve.

Table 3. Simulation and measurement data comparison for GGMOS model.

Parameter	Simulated	Measured	Difference (%)
V_{t1}	8.780 V	8.580 V	2.3
I_{t1}	0.022 A	0.03 A	26,6
V_h	6.680 V	7.08 V	5.6
I_h	0.209 A	0.22 A	5.0
V_{t2}	9.710 V	10.100 V	3.8
I_{t2}	1.201 A	1.220 A	1.6

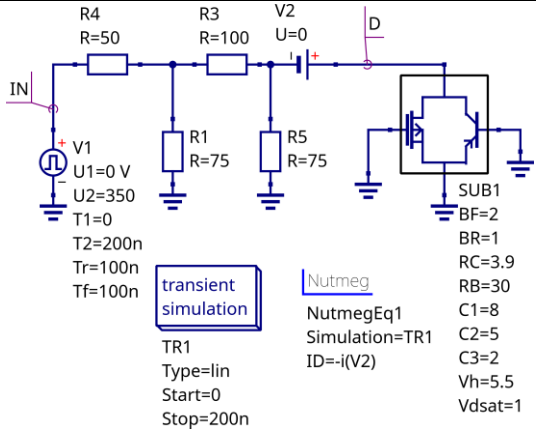

Fig. 9. GGMOS model transient testbench schematic.

The voltage V_{DUT} and current I_{DUT} waveforms across the device under test are shown in the Fig. 10. The device is triggered on the leading edge and turned off at the trailing edge of the pulse.

The device IV-curve may be extracted not only from DC simulation, but also from transient. The Fig. 11 shows the device current plotted versus device voltage. The hysteresis could be seen in this

curve. This could be explained by different turn-on and turn-off voltage of the GGMOS device. The extraction of hysteresis data for GGMOS device requires a series of TLP measurement with different pulse rise time.

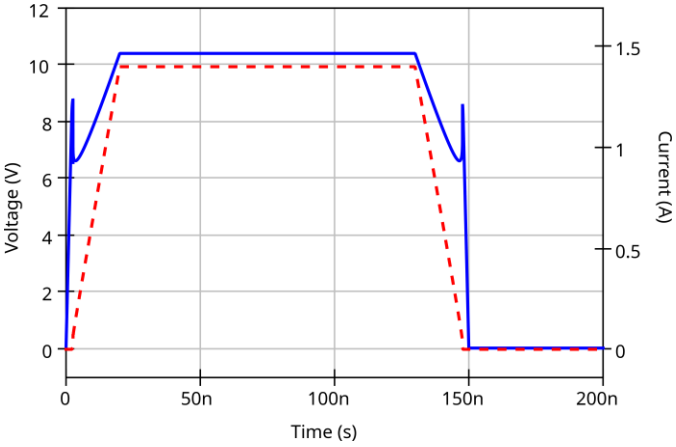

Fig. 10. Voltage (solid curve) and current (dashed curve) GGMOS device transient waveforms.

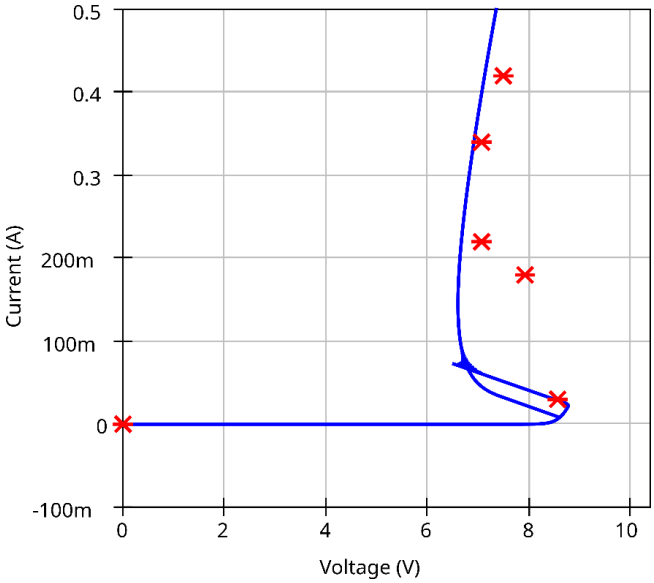

Fig. 11. Transient IV-curve of the GGMOS device (solid curve) and measured TLP quasi-static IV-curve (stars).

5. Conclusion

The macromodels for two ESD protection devices (ESD diode and GGMOS) were developed in the presented research. These devices are the most commonly used in the modern microelectronics. The presented macromodels were designed using the open-source circuit simulation tools (Qucs-S and Ngspice) that allows to use it with open process design kits (PDKs) [13]. Some measures were undertaken to improve the simulation convergence using the proposed models. The developed macromodels show a good matching of the measurement and simulation data and allow to estimate both DC and transient behavior of the ESD protection circuit. This allows to extent the SPICE simulation and estimate the ESD robustness of the IC at the early design stage. The disadvantage of

the implemented models is a sufficient complex extraction procedure that requires fine adjustment a number of the fitting coefficients.

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